



Guru Aanklan

**GRAND
TEST**

**ELECTRONICS PAPER - II
HSC DIGITAL ELECTRONICS
PAPER - [A]**

SOLUTIONS

Q. 1A Sol.

- 1) (C) 8
- 2) (D) EX-ORgate
- 3) (C) magnetic tape
- 4) (B) one half of its input frequency

Q. 1B.

Sol.1 (A) $(11010)_2 - (11011)_2$

$$\begin{array}{r}
 11010 \quad 11010 \\
 -11011 \quad +001000 \text{ (1's Comp. of 11011)} \\
 \hline
 -011101 \quad 100010
 \end{array}$$

As last carry is absent, answer is negative and in 1's complement form.

Sol. = -011101

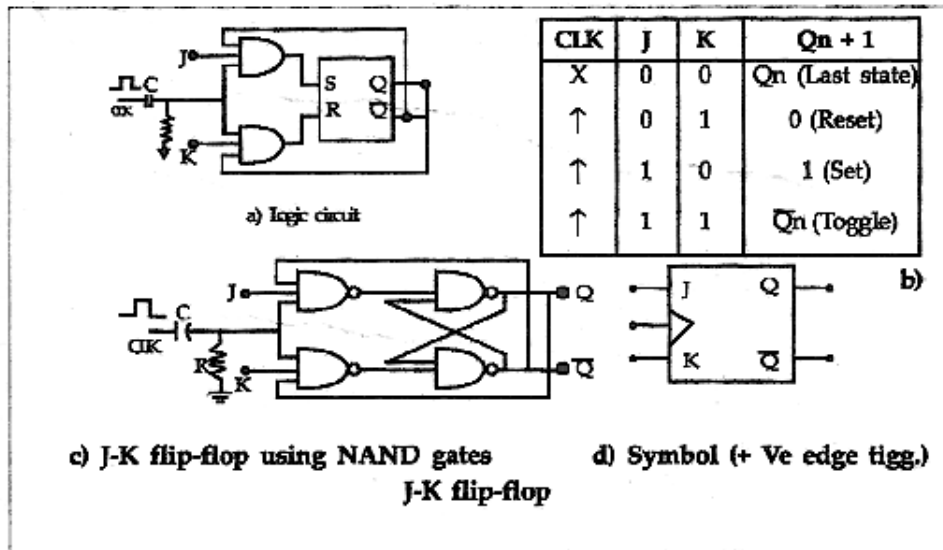
(B) $(11011)_2 - (01101)_2$

$$\begin{array}{r}
 11011 \\
 + \quad 10010 \quad \text{(1's Comp. of 01101)} \\
 \hline
 11011 \quad 101101 \\
 -01101 \\
 \hline
 01110 \quad \text{EAC + 1} \\
 \hline
 01110
 \end{array}$$

As EAC is present, answer is positive.

Sol. = 01110

Sol.2 J - K Flip-flop :



J and K are called ‘control inputs’ because they can determine what the flip-flop does when a positive clock edge arrives. RC circuit is a differentiator circuit having short time constant and it converts rectangular clock pulse into narrow spikes. Because of AND gates, the circuit in fig. (a) is positive edge triggered. In fig. (c) also positive edge triggering is used. The circuit is inactive when the clock is low (0), high (1) or on its negative edge (↓) and output remains in last state. When J and K are low both AND gates are disabled. Therefore clock pulses have no effect and output remains in last state. When J = 0 and K = 1, On the positive clock edge, lower gate is enable and it passes a reset trigger. Therefore flip-flop is Reset (0). When J = 1 and K = 0, upper gate is enable and it passes a set trigger on next positive clock edge. Therefore flip-flop is set (1). When J = 1 and K = 1, it is possible to set or reset the flip-flop. If Q is high, lower gate passes a reset trigger on positive clock edge and Q becomes low (0). If Q is low, upper gate 1, complement of last state is obtained. This is called ‘**Toggling**’. Toggling more than once during a positive clock edge is called ‘**Racing**’. This is avoided due to propagation delay time. Use-In counters.

Sol.3. EBCDIC (Extended Binary Coded decimal Interchange Code)

It is an 8-bit code allowing a maximum of 256 characters to be represented. It is an improvement over ASCII. Its primary use is in IBM and IBM compatible equipments.

EBCDIC code is an alphanumeric code which can be used to represent numbers, letters and special symbols.

e.g. 11000001 (A), 11010100 (M)
11110100 (4), 01001110 (+)

Q.2A

Sol.1 Register- A register is a group of flip-flops that can be used to store a binary number.

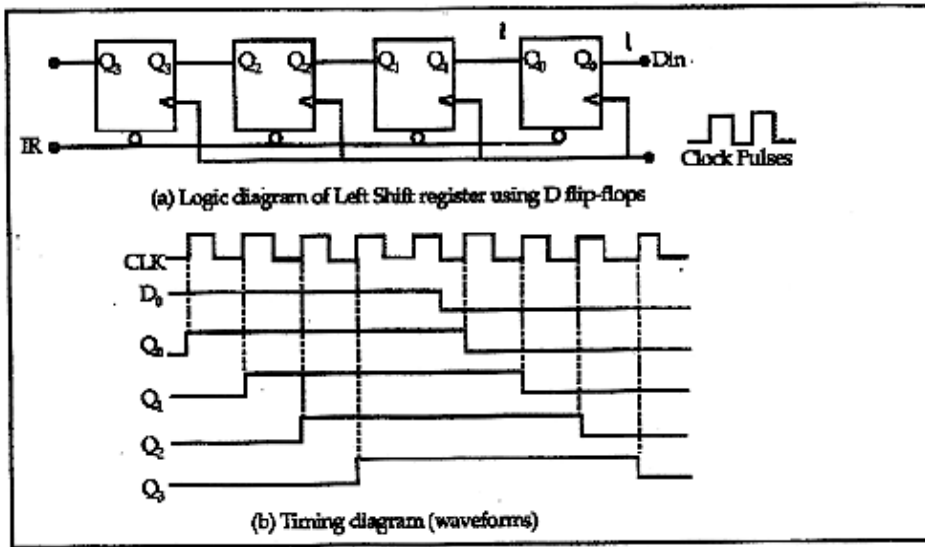
There must be one flip-flop for each bit in the binary number.

Applications of registers:

- 1) To store data in digital system.
- 2) Used to convert a serial data to a parallel form and vice versa.
- 3) Data in a register can be shifted to left or right by any number of bit positions which is equivalent to multiplication or division by 2, 4 etc.
- 4) Desired delay in the arrival of a data bit stream can be introduced.
- 5) Rate of transmission of data can be changed with the help of a shift register.

Sol.2

4 bit left shift register



4-bit left shift register consists of D flip-flops. D_{in} is the data input to the first flip-flop Q_0 sets up the second flip-flop, Q_1 the third and so on. When the next positive clock edge strikes, the stored bits move one position to the left.

Initially all flip-flops are cleared. Therefore, the stored word becomes $Q = Q_3 Q_2 Q_1 Q_0 = 0000$.

With $D_{in} = 1$ on the arrival of the first rising clock edge the stored word becomes $Q = 0001$.

Now $D_0 = 1$ and $D_1 = 1$. on the second positive edge Q becomes 0011.

On the positive edge of third clock pulse $Q = 0111$.

On the fourth positive clock edge $Q = 1111$.

Now as long as $D_{in} = 1$, this stored word remains unchanged.

Suppose D_{in} is now changed to 0. Then successive clock pulses produce following register contents. $Q = 1110$ $Q = 1100$ $Q = 1000$ $Q = 0000$

As long as $D_{in} = 0$, subsequent clock pulses have no further effect. Shift-left operation is essential for certain arithmetic and logic operations used in microcomputers.

CLK No.	Din	Q_3	Q_2	Q_1	Q_0
1	1	0	0	0	1
2	1	0	0	1	1
3	1	0	1	1	1
4	1	1	1	1	1
5	1	1	1	1	1
6	0	1	1	1	0
7	0	1	1	0	0
8	0	1	0	0	0
9	0	0	0	0	0

Sol.3. (A) $(25)_{10} = 25 \div 2 = 12$ with a remainder of 1
 $12 \div 2 = 6$ with a remainder of 0
 $6 \div 2 = 3$ with a remainder of 0
 $3 \div 2 = 1$ with a remainder of 1
 $1 \div 2 = 0$ with a remainder of 1
 $\therefore (25)_{10} = (11001)_2$

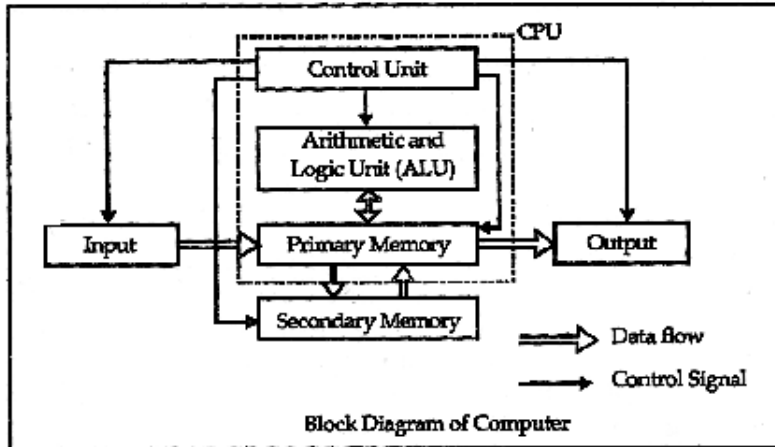
(B) $(C5)_{16} = C(16^1) + 5(16^0) = 12(16) + 5(1)$
 $= 192 + 5 = 197$
 $\therefore (C5)_{16} = (197)_{10}$

(C) $(69)_{10} = (0110\ 1001)_{BCD}$

(D) $(B\ 7C)_{16}$

	7	C
B	↓ 7	↓ 12
↓ 11	0111	1100
1011	$\therefore (B\ 7C)_{16} = (1011\ 0111\ 1100)_2$	

Q.2 B
Sol.1.



The computer consists of five units : 1) Input 2)Output, 3)Primary Memory, 4)Control and 5)ALU. The input and output devices are called 'Peripherals' as they surround the remaining blocks. The ALU, memory and control unit are called '**Central Processing Unit**' (CPU). A computer system is complete even without the secondary memory which only increases the memory capacity. **Input devices** convert data and program instructions into a format that is understandable by the computer. Input unit should be capable of accepting the data and program at fast speed. The most popular input device in a microcomputer is the keyboard. Direct entry input devices like the digitizer and the mouse are popular devices used for desk top publishing work. **CPU-** The central processing unit is the brain of the computer. It temporarily stores current data and program instructions and acts on them as directed. **The arithmetic and logic unit (ALU)** does all the arithmetic computations and logical operations. The arithmetic computations involve performing addition, subtraction, multiplication and

division operations while logical operations involve comparisons. A computer can solve complex mathematical problems within a short interval of time because of arithmetic algorithm.

The control unit (CU) directs the sequence of CPU operations. This unit directs the entire computer system to carry out and execute the program instructions. It co-ordinates the activities of input and output devices.

The primary memory holds the program instructions for the program to be executed, the input data to be processed and the intermediate results of any calculations when the processing is being done. e.g. RAM, ROM, PROM etc.

The output devices convert the processed data or results into a user understandable form. e.g. printers & plotters, magnetic disk, magnetic tape, computer output microfilm (COM) etc.

Secondary memory- The working storage inside the CPU is often limited in size and thus is not able to hold all the data ready to be processed. Secondary or auxiliary storage is often found physically outside the computer system and is cheaper form of storage media. e.g. Magnetic disks & magnetic tapes.

Address- In a computer system, each memory location of the primary memory or each peripheral is assigned a binary number with which it can be identified. This is known as its 'Address' This binary number may be 4,8,16 or more no. of bit long. In general if r is the base of the number system chosen, n is the number of address lines and m the number of memory locations to be addressed, then $r^n = m$ The data flow and control signals are shown in figure.

Sol.2 Shift Registers- The registers in which data is entered or/ and taken out in serial form are referred to as 'Shift Registers'. Bits are shifted in the flip-flops with the occurrence of clock pulses either in the right direction (right shift) or in the left direction (left shift). Sometimes it is necessary to shift data to the right and/ or to the left. A binary number can be divided by two by shifting it one stage to the right. In this process the least - significant bit (LSB) is lost unless additional circuitry is used to preserve it which causes an error of 0.5 if the number is odd. A number stored in a shift register can be multiplied by two by shifting one stage to left. For example if the number $011_2 = 3_{10}$ is shifted left one place, the register contains $110_2 = 6_{10}$.

The bits in a binary number (data) can be moved from one place to another in either or two ways.

1) In '**Serial Shifting**' the data is shifted 1 bit at a time in a serial (fashion). 2) In '**Parallel Shifting**' all the data bits are shifted simultaneously.

Type of Registers:

- | | |
|----------------------------------|-------------------------------------|
| 1) Serial in-Serial out (SISO) | 2) Serial in- Parallel out (SIPO) |
| 3) Parallel in-Serial out (PISO) | 4) Parallel in-Parallel out. (PIPO) |

Q.3 A

Sol.1 Counter - Counter is a subsystem in digital electronics which is driven by a clock pulse. Counters are mainly used to count the number of clock pulses. But as clock pulses occur at known intervals, counters can be used for following applications also.

Applications of Counters:

For frequency division

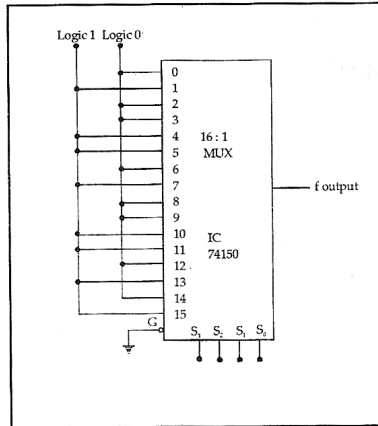
- 1) For frequency division
- 2) Measurement of time
- 3) In digital voltmeter
- 4) In analog to digital converters
- 5) Measurement of frequency
- 6) Measurement of time interval between two event.

Types of Counters:

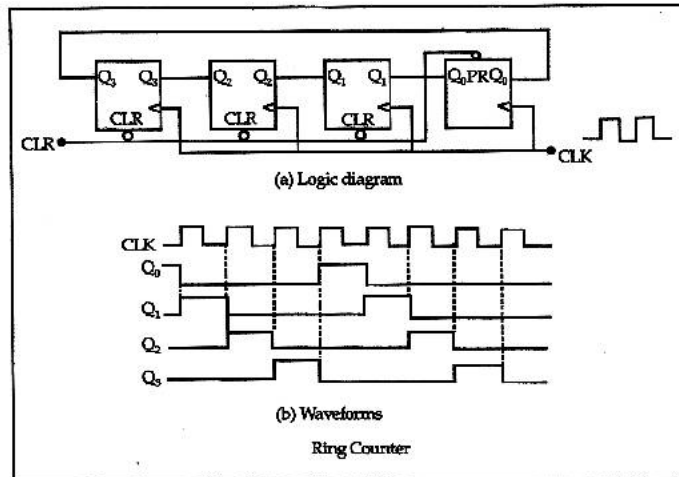
- 1) Ripple or Asynchronous or Serial Counter

- 2) Parallel or Asynchronous Counter
- 3) Combination Counters.

Sol.2 As the given multiplexer IC has inverted inputs, terminals 0, 2, 3, 6, 8, 9, 12, 14 should be connected to logic zero and terminal 1, 4, 5, 7, 10, 11, 13, 15 should be connected to logic one



Sol.3 Ring Counter using D flip-flops



Ring counter can be constructed by using D flip-flops. Any external data input is not applied. Q_0 is connected to D_1 , Q_1 to D_2 , Q_2 to D_3 and Q_3 back to D_0 . Initially a low pulse is applied to PR input of first flip-flop and CLR inputs of remaining flip-flops.

Therefore stored word $Q = Q_3 Q_2 Q_1 Q_0 = 0001$.

On the positive edge of first clock pulse $Q = 0010$.

On the positive edge of Second clock pulse $Q = 0100$.

On the positive edge of third clock pulse $Q = 1000$.

On the positive edge of fourth clock pulse $Q = 0001$.

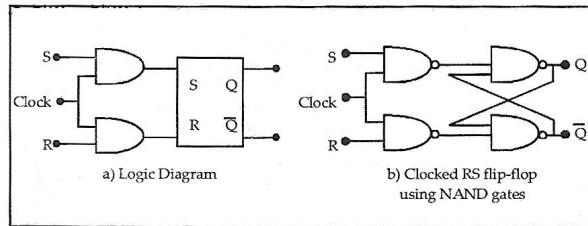
Thus a cycle is completed. The stored bit follows a circular path, moving left through the flip-flops until the final flip-flop sends it back to the first flip-flop. Therefore, this circuit is called as a Ring counter. This action is called as Rotate left.

Truth table of ring counter

Clock	Q3	Q2	Q1	Q0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0
4	0	0	0	1

Q.3.B

Sol.1 Clocked RS Flip-Flop.



R	S	Q	Action
0	0	Last state	No change
0	1	1	Set
1	0	0	Reset
1	1	Forbidden	Race

The addition of two AND gates will result in a flip-flop that can be enabled or disabled. When the clock input is low, the AND gate output is 0. The latch is ‘disabled’.

When CLK input is high, data at R and S input will be transmitted directly to the output. The latch is ‘enabled’. The output will change according to input when the CLK is high. When CLK goes low, output will retain the information on input when high to low transition takes place.

We consider two instants in time : the time before the CLK goes low as Q_n and the time just after CLK goes low as Q_{n+1} .

If $S = 0, R = 0$ and CLK is high, $Q_n = Q_{n+1}$. Therefore there is no change in the last state.

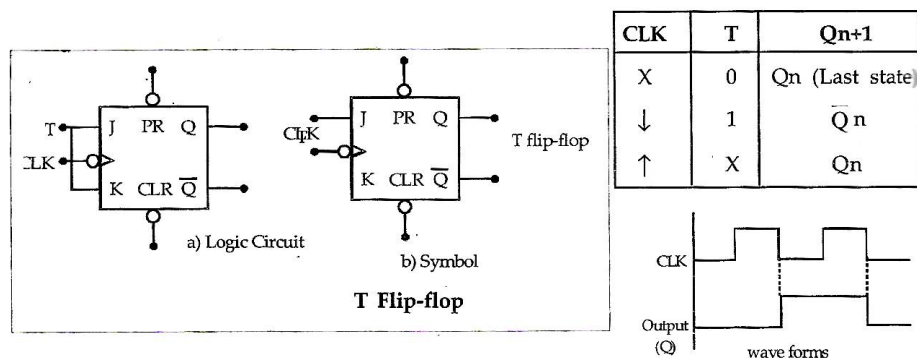
If $S = 0, R = 1$ at the end of CLK pulse, $Q_{n+1} = 0$ (Reset).

Similarly for $S = 1$ and $R = 0$, $Q_{n+1} = 1$ (Set).

But $S = 1$ and $R = 1$ can not be allowed, and this state is forbidden.

Disadvantages (draw backs) of R-S flip-flop :-

Sol.2 T (Toggle) Flip-Flop:



In a JK flip-flop if $J=K$, T flip-flop is formed, It has only one input called as T input. If $T = 1$ ($J = K = 1$), it acts as a toggle switch. On negative edge of each clock pulse, the output Q changes (toggles). Toggle means switching to the opposite state, Positive edge triggered T-FF also can be constructed.

T flip-flop divides the clock frequency by two. For example, if clock frequency is 2 kHz, output (Q) frequency is 1 kHz. Use-In counters.

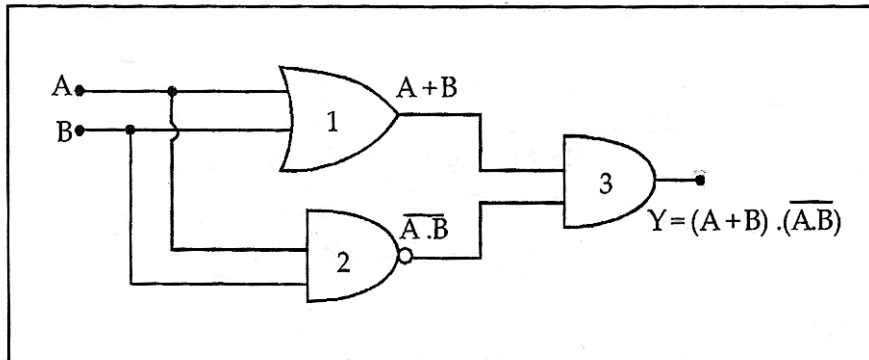
Q. 4.A

Sol.1 In volatile memory the contents of the memory vanish as the power to the computer is switched off.

Type of volatile memory:

- i) **Static RAM :** This uses bipolar or MOS flip-flops. Data is retained indefinitely as long as power is applied to the flip-flops.
- ii) **Dynamic RAM :** This uses MOSFETs and capacitors that store data. As the capacitor charge leaks off, the stored data must be refreshed (recharged) every few milliseconds.
- iii) **Cache memory :** This is very fast semiconductor memory which improves the overall performance of the computer. This memory is also called as ‘scratchpad memory’.

Sol.2.



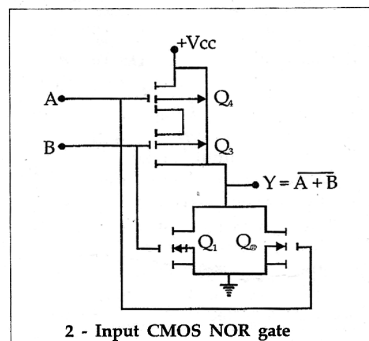
Logic diagram

Sr. No.	Name of Gate
1.	OR
2.	NAND
3.	AND

Truth table :

A	B	A + B	$\overline{A.B}$	Y
0	0	0	1	0
0	1	1	1	1
1	0	1	1	1
1	1	1	0	0

Sol.3 Explain the working of CMOS NOR gate with necessary circuit diagram



In CMOS NOR gate, NMOS (n - channel) drivers are connected in parallel and PMOS (p -channel) loads are connected in series.

Generally CMOS ICs require power supply from 3 to 15 V. The output is High when Q_3 and Q_4 are ON. The output is Low when Q_1 or Q_2 in ON.

Q.4.B

Sol.1 CMOS NAND gate -

N - channel MOS conducts when its gate to source voltage is positive

P - channel MOS conducts when its gate to source voltage is negative.

Inputs		State of MOS devices				Out Put
A	B	Q1	Q2	Q3	Q4	Y
0	0	off	off	on	on	1
0	0	on	off	on	off	1
1	0	off	on	off	on	1
1	1	on	on	off	off	0

In the COMS NAND gate, the NMOS drivers are connected in series and the PMOS load are connected in parallel. The operation of NAND gate can be understood from the table. The output is High when Q_3 or Q_4 or both are ON. The output is Low when Q_1 and Q_2 are ON.

Sol.2 Types of Digital to Analog (D/A) Converters : (DAC)

1) Weighed - Resistor D/A converter (Primary weighted DAC)

2) R-2R Ladder D/A converter.

Type-Weighted Resistor D/A converter:

Principle - For conversion of a digital signal into an equivalent analog signal the n digital voltage levels should be changed into one equivalent analog voltage. This can be done by designing a resistive network that will change each digital level into an 'equivalent binary weighted' voltage or current.

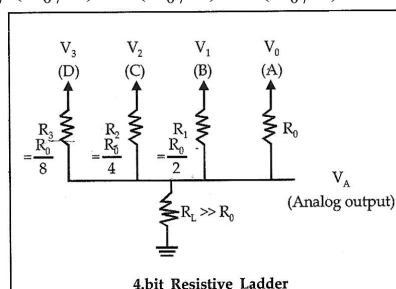
Working - The resistive divider can be built to change a digital voltage into an equivalent analog voltage. **Following criteria can be applied to this divider :**

- 1) There must be one input resistor for each digital bit.
- 2) Beginning with LSB, each following resistor value is one half the value of previous resistor, e.g. R, R/2, R/4, R/8 etc.
- 3) The full- scale output voltage is equal to the positive voltages of the digital input signal.
- 4) The LSB has a weight of $1/2^n - 1$, where n is no. of input bits.
- 5) The change in output voltage due to a change in the LSB is equal to $v(2^n - 1)$ where V is the digital input voltage level.
- 6) The output voltage V_A can be found by using following modified form of Millman's theorem:

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \dots V_{n-1} 2^{n-1}}{2^n - 1}$$

where $V_0, V_1, V_2, \dots, V_{n-1}$ are digital input voltage levels (0 or V) and n is the number of input bits. For 4 bit resistive ladder:

$$V_A = \frac{V_0/R_0 + V_1(R_0/2) + V_2(R_0/4) + V_3(R_0/8)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4) + 1/(R_0/8)}$$



Digital Input = 0 = 0 V 1 = 15v, (Analog Output)				
(MSB) D	C	B	(LSB) A	V_A (volts)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

In 4-bit D/A converter, 4 resistors are used. Beginning with LSB their values are R_0 , $R_0/2$, $R_0/4$, $R_0/8$. Resistance R_L is large enough so that it does not load the divider network.

The LSB has a weight of $1/(2^n - 1) = 1/2^4 - 1 = 1/15$.

Disadvantages- (Drawbacks).

- 1) Each resistor in the network has a different value e.g. R_0 , $R_0/2$, $R_0/4/8$ etc. The values of these resistors should be very accurate. In absence of precision resistors, the output will not be a faithful analog equivalent.
- 2) As precision resistors are used. cost is more.
- 3) Resistors of appropriate smaller value are not easily available and the resistance may be affected by changes in temperature.
- 4) The resistor used for the MSB is required to handle a much greater current than that used for the LSB resistor.

In practice, instead of a high value. R_L , an operational amplifier as an adder is used.

Q.5A

Sol.1 Type 3 : Successive Approximation Analog to Digital Converter:

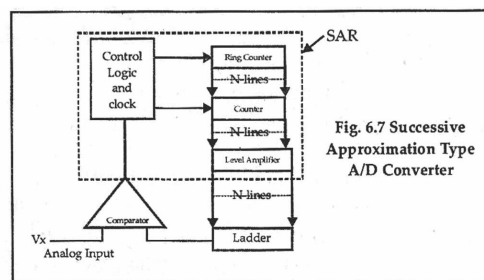
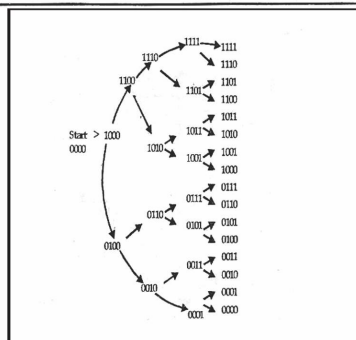


Fig. 6.7 Successive Approximation Type A/D Converter



If multiplexing is required, the successive approximation A/D converter is most useful. It compares the analog input to a DAC reference voltage that is repeatedly divided in half.

The counter is first reset to all 0s and MSB is then set. The MSB is then left in or taken out by resetting the MSB flip-flop depending on the output of the comparator. Then second MSB is set in and a comparison is made to determine whether to reset the second MSB flip-flop. This process is repeated to LSB and at this time the desired number is in the counter. A ring counter is used for flip-flop at a time, beginning with the MSB.

This method is the process of approximating the analog voltage by trying 1 bit at a time beginning with the MSB. This operation is shown in fig. 6.8 Each conversion takes the same time and requires one conversion cycle for each bit. Thus total conversion time is equal to the number of bits (n) times the time required for one conversion cycle.

The blocks shown inside the dashed line in fig. 6.7 can be constructed on a single MSI chip. this chip is called as 'Successive-Approximation Register' (SAR). e.g. Motorola 14549 is a 8-bit SAR.

This type of A/D converter can be used for digital voltmeters.

Sol.2 Type 2 : Counter Type Analog to Digital Converter:

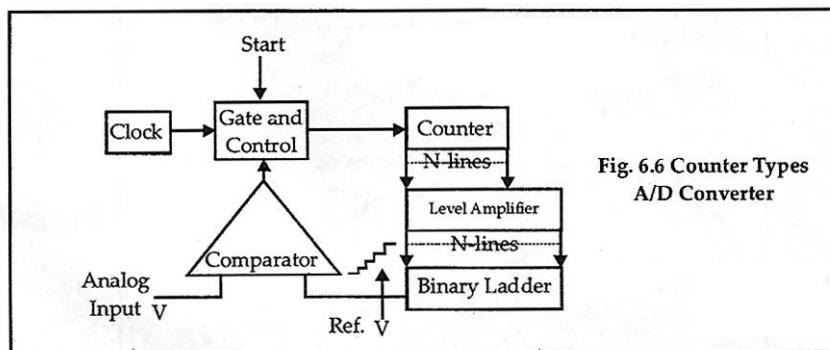


Fig. 6.6 Counter Type A/D Converter

If the reference voltage to which the analog input is to be compared is variable the number of comparators can be reduced to only one. This principle is used in counter type A/D converter. The counter, level amplifiers and binary adders form the D/A converter. First, the counter is reset to all 0s. When a convert signal appears on the start line, the gate opens and clock pulses are allowed to pass through to the input of the counter. The counter advances through its normal binary count sequence, and the staircase waveform is generated at the output of the ladder. This waveform is applied to one side of the comparator and analog input V is applied to the other side. When the reference V equals or exceeds the input analog voltage the gate is closed and the counter stops. The number stored in the counter is now the digital equivalent of the analog input voltage.

This circuit can be considered as a closed-loop control system. An error signal is generated at the output of the comparator by taking the difference between the analog input signal and feedback staircase reference signal. The error is detected by the control circuit and the clock is allowed to reduce the error signal by increasing the feedback voltage. When error is zero, feedback voltage is equal to analog input signal. The control circuit stops the clock from advancing the counter and system comes to reset.

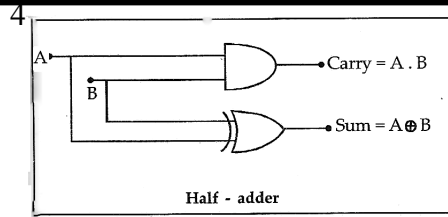
Advantages -1) High resolution.

2) Requires only one comparator

Drawback- Conversion time required is longer and it depends on clock frequency.

Sol.3 Half-adder : Half-adder is a logic circuit which can add two binary digits at a time. It consists of an exclusive-OR gate and an AND gate.

The output of XOR gate is the sum and output of AND gate is the carry.



A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

1) When A = 0 & B = 0
 Sum = $A \oplus B = 0 \oplus 0 = 0$
 Carry = $AB = 0.0 = 0$

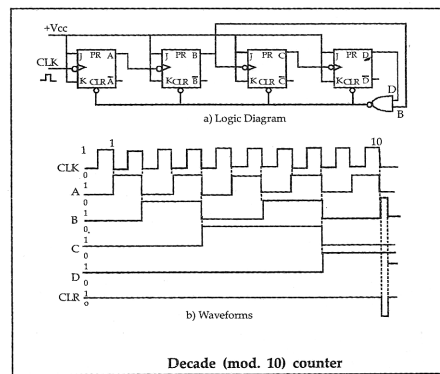
2) When A = 0 & B = 1
 Sum = $0 \oplus 1 = 1$,
 Carry = $0.1 = 0$

2) When A = 1 and B = 0
 Sum = $1 \oplus 0 = 1$
 Carry = $1.0 = 0$

2) When A = 1 and B = 1
 Sum = $1 \oplus 1 = 0$,
 Carry = $1.1 = 1$

Q.5.B

Sol.1 Decade (Mod-10) Counter: (Asynchronous)



Clock pulses (Count)	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0

By using 4 negative-edge triggered JK flip-flops a Mod-16 counter can be constructed. A decade counter can be constructed from Mod 16 counter by skipping six states. Such counter is called as Modified counter. Feedback is used for skipping unwanted states. A clock signal drives A flip-flop. The output of A drives the B flip-flop. The output of B drives

the C flip-flop and C drives the D flip-flop. All J and K inputs are connected to + Vcc. Each flip-flop will toggle with a negative transition at its clock input.

Let's assume that all flip-flops are initially reset to zero output condition DCBA = 0000.

When first clock pulse comes in, flip-flop A changes state on its negative edge \therefore DCBA = 0001. When second clock pulse comes in, on its negative edge. A change from 1 to 0. This being a negative change B changes from 0 to 1 \therefore DCBA = 0010. Similarly on negative edge of third clock pulse, DCBA = 0011.

Thus the output condition of the flip-flops is a binary number equivalent of the number of clock-pulses received. The output conditions are shown in the truth table.

After nine clock pulses, DCBA = 1001.

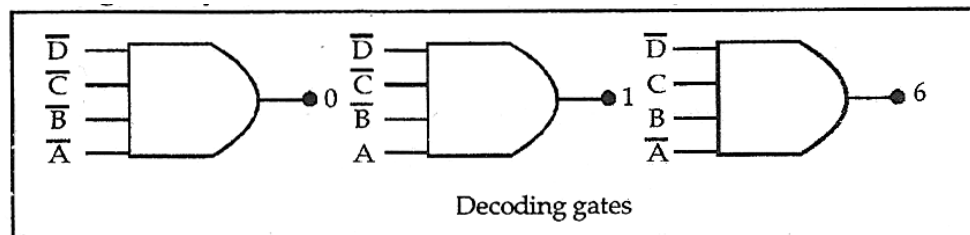
On the negative edge of 10th clock pulse. A changes from 1 to 0. Therefore B change from 0 to 1. This being a positive change flip-flops C and D are not affected \therefore DOBA = 1010.

But this is **momentary state**.

The NAND gate provides a Reset (clear) pulse to all flip-flops as

B = 1 and D = 1. Therefore the counter resets to 0000. Thus remaining six states are skipped out and the counter becomes Mod-10 (Decade) counter.

10 decoding gates can be used to represent the output in decimal code. 10 four-input AND gates are required. For example, the AND gate with inputs, $\bar{A}, \bar{B}, \bar{C}$ and \bar{D} represents 0. Its output is high only for count 0. Similarly the AND gate with inputs D, \bar{C}, \bar{B}, A represents 9. Its output is high only for count 9. Some decoding gates are shown below:



Sol.2 Types of Secondary Memory Devices :

- A) Direct access secondary storage-
 1) Floppy disk, 2) Hard disks 3) CD ROM
 B) Sequential access secondary storage-Magnetic tape.

OR

Q.5 A

Sol.1 Logic Family : Based on the semiconductor devices, digital integrated circuits are made and are commercially available. Many complex digital functions have been realized in a variety of forms and each form is referred to as a Logic family.

Types of logic families :

A) Unipolar Logic families :

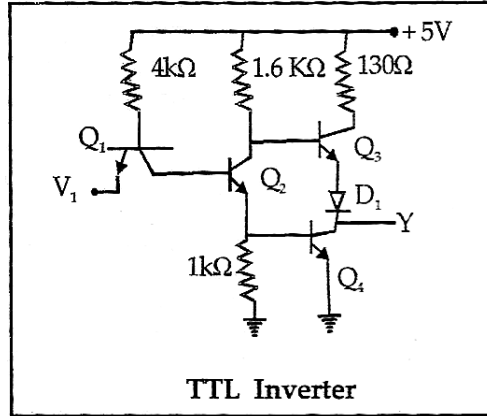
- 1) PMOS, 2) NMOS and 3) CMOS

B) Bipolar Logic families -

- a) Saturated Bipolar Logic families -
 1) Resistor - Transistor Logic (RTL)
 2) Direct - Coupled Transistor Logic (DCTL)
 3) Integrated - Injection Logic (I²L)
 4) Diode - Transistor Logic (DTL)

- 5) High - Threshold Logic (HTL)
- 6) Transistor - Transistor (TTL)
- b) Non- saturated Bipolar Logic (TTL)
- 1) Schottky TTL, 2) Emitter-Coupled Logic (ECL)

2.Sol. TTL Inverter –



V_1 and V_0 are the input and output voltage respectively. When V_1 is low, Q_1 saturates, Base voltage of Q_2 drops to zero. Therefore Q_2 and Q_4 go to cutoff condition. Hence high output is obtained. When V_1 is high, collector diode of Q_1 goes into saturation. Q_2 and Q_4 go into saturation and produce a low output.

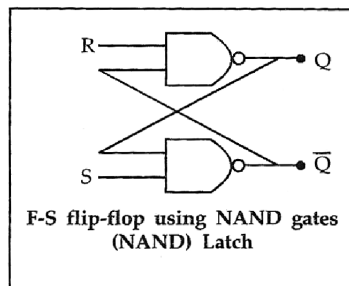
Worst -case input voltages are $0.8V$ is for low and $2V$ for high. This means that low input may be from $0V$ to $0.8V$ and high input may be from $2V$ to $5V$.

Similarly worst - case output voltages are $0.4 V$ for low and $2.4 V$ for high state.

Truth V_1	Table V_0
0	1
1	0

For example, TTL IC 7404 is Hex Inverter.

3.sol. 1. Bit Memory Cell :



A basic digital memory cell consists of two NAND gates used as inverters. The output of G_1 is connected to the input of G_2 as A_2 and the output of G_2 is connected to the input of G_1 as A_1 .

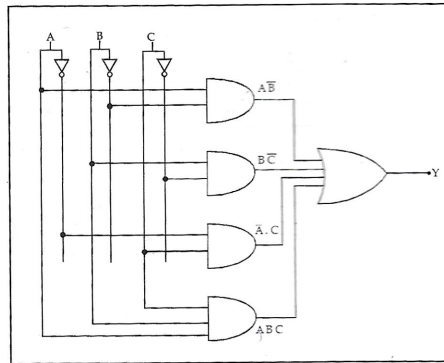
Let us assume the output of G_1 to be $Q = 0$. Therefore input of G_2 i.e. $A_2 = 0$. the output of G_2 will be $\bar{Q} = 1$, which makes $A_1 = 1$ and $Q = 0$ which confirms our assumption. Similarly it can be shown that if $Q = 1$, then $\bar{Q} = 0$

Therefore we can conclude that :

- 1) The output Q and \overline{Q} are always complementary.
- 2) The circuit has two stable states. In one stable state $Q = 1$ which is called set state and in other stable state $Q = 0$ which is called as Reset state.
- 3) If the circuit is in 1 state – bit (binary digit) of digital information. This information is locked or latched in this circuit. Therefore this circuit is also called as a ‘Latch’
Two NAND gates can be added to this circuit, to have the provision for entering data in form of S and R inputs, Therefore the memory cell can be set (1) or reset (0)

Q.5B

Sol.1 Logic Diagram



$$Y = \overline{A}B + B\overline{C} + \overline{A}C + ABC$$

Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Sol.2 For 4 bit $R - 2R$ ladder,

$$\text{analog output voltage} = V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3}{2^n}$$

where V_0 correspond to LSB and V_3 to MSB.

since $0 = 0V$ and $1 = 32V$,

$$\begin{aligned} V_A &= \frac{32x2^0 + 32x2^1 + 0 + 2^2 + 32x2^3}{2^4} \\ &= \frac{32 + 64 + 256}{16} \\ &= \frac{352}{16} = 22V \end{aligned}$$